EE 505
Homework 2
Spring 2025
Due Friday Feb 28

**Problem 1** An expression was derived for the quantization noise in an ADC whereby it was assumed that the output could change instantaneously to a new quantization value whenever the input transitioned across a break point of the ADC. With either a full-scale sinusoidal or triangle input, it was shown this quantization noise was $X_{LSB}/\sqrt{12}$. Correspondingly, if the ADC is clocked at a given clock rate and the resolution of the ADC is infinite, there will be a difference between the actual continuous-time ADC input and the interpreted quantized ADC output. This difference can be called the time quantization noise. Finally, if an ADC has finite resolution and is clocked, both time and amplitude quantization errors will be present.

a) What is the time quantization error for an ADC that is clocked at a frequency that is 10 times the signal frequency (assume the input is a full-scale sinusoidal waveform)? How is this quantization error distributed?

b) How does the time quantization error change as the clock frequency increases or decreases?

c) What is the combined time quantization error and amplitude quantization error for an ideal 12-bit ADC that is clocked at a frequency that is 10 times the signal frequency?

**Problem 2** An ADC is to be used in an electronic scale that has a full-scale input of 100LBs and an accuracy requirement that the error be no more than 0.5% of full scale and no more than 1 oz for inputs between 0Lb and 2LB.

a) How many bits of resolution are needed in the ADC to meet these specifications if the ADC is ideal?
b) What resolution, INL, and DNL specifications are needed to meet these requirements?
c) Specify a commercial ADC that will meet (but not substantially exceed) these requirements.

(you may assume that offset and gain adjustments can be made on your ADC)

**Problem 3** If a 12-bit DAC has a 25% duty cycle (DAC output returns to 0 over 75% of each clock period).

a) Determine the signal output and the SNR if the DAC is to output a maximum-amplitude sine wave. Assume the clock frequency of the DAC is 25 times the signal frequency and that a zero-order sample and hold is used with a 25% duty cycle. The Boolean input to the DAC should be the signal that would be obtained from an ideal 12-bit ADC that samples the sinusoidal input signal.
b) What is the SFDR and the THD (through the first 4 harmonics) for this DAC?

**Problem 4** If a 6-bit DAC has a DNL of at most 0.1LSB, what is the worst possible INL (in LSB) that this DAC could have? (Define $X_{LSB}=\frac{X_O\left(2^n\text{-}1\right)\text{-}X_O(0)}{2^n\text{-}1}$ )

**Problem 5** Consider a 14-bit ADC with a reference voltage of 1V. What will be the signal to quantization noise error if a sinusoidal input with a peak-to-peak value of 0.1V and an offset of 0.2V is applied to the input? How does that compare to the signal to quantization noise if the input has a peak-to-peak value of 1V and an offset of 0.5V?

**Problem 6** An important theorem was stated in class and is given below. Prove this theorem. You may use appropriate reference to help with this proof but the proof you give should be rigorous.

Theorem: If n(t) is a random process, then for large T,

$$V_{RMS}=\sqrt{\frac{1}{T}\int_{t_1}^{t_1+T} n^2(t)dt}\ =\sqrt{\sigma_n^2+\mu_n^2}$$

**Problem 7** An important theorem was stated in class and is given below. Prove this theorem. You may use appropriate reference to help with this proof but the proof you give should be rigorous.

**THEOREM: If $N_P$ is an integer and the periodic signal x(t) is band limited to $f_{MAX}$, then**

$$|A_m|=\frac{2}{N}|X(mN_P+1)| \qquad 0\le m\le h\text{-}1$$

**and** $X(k)=0$ **for all k not defined above**

**where** $\langle X(k)\rangle_{k=0}^{N-1}$ **is the DFT of the sequence** $\langle x(kT_S)\rangle_{k=0}^{N-1}$

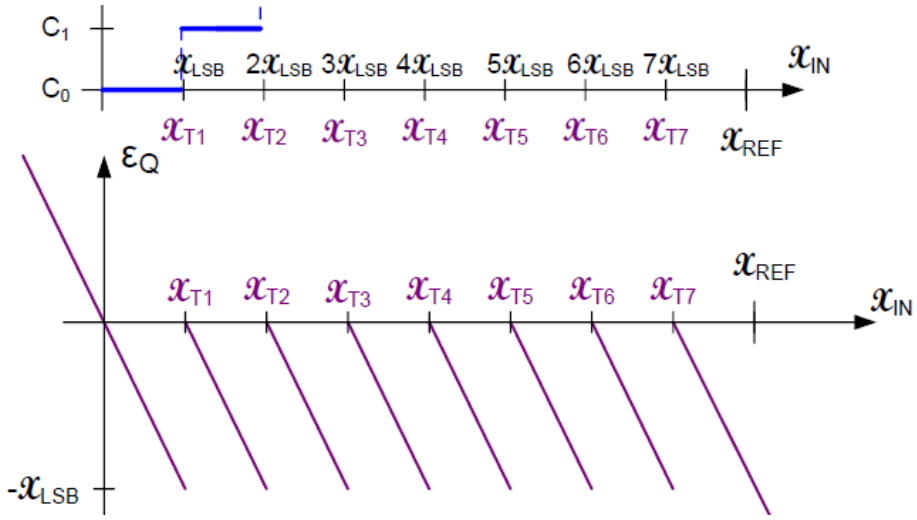
**f = 1/T,** $f_{MAX}=\frac{f}{2}\cdot\left[\frac{N}{N_P}\right]$ **, and** $h=\mathrm{Int}\left(\left[\frac{N}{2}\text{-}1\right]\frac{1}{N_P}\right)$

**Problem 8** Assume a 12-bit DAC with a $V_{REF}$ of 1V has outputs that lie on the locus $V_{OUT}=0.01+0.98x+.01x^2$ where x is the interpreted value of the digital input code. Determine the following parameters for the DAC: DNL, INL, THD for a full-scale sinusoidal input, SFDR, and the ENOB. For those parameters that are dependent upon

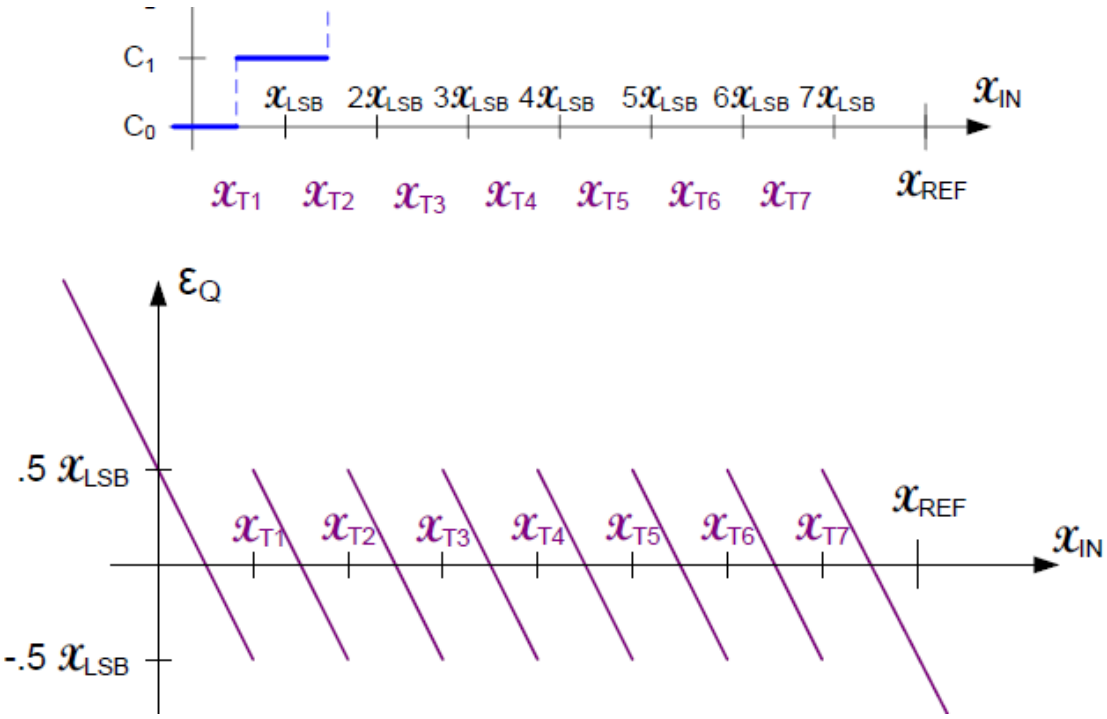
spectral characteristics, the Boolean input to the DAC should be the signal that would be obtained from an ideal 12-bit ADC that samples the distorted input signal. Assume the clock frequency on the DAC (and correspondingly the ideal sampling ADC) is arbitrarily high so that the output of the DAC is a waveform that is continuous at all times except at times when transitions occur in the input codes.

Problem 9 The breakpoints of an ideal ADC can be placed in different locations. In the first scenario shown below the breakpoints are at integer multiples of $X_{LSB}$. In the second scenario the first breakpoint is at $X_{LSB}/2$ and the remainder are equally spaced $X_{LSB}$ apart. The corresponding quantization errors are shown below and are different. In the calculation of quantization noise, the location of the breakpoints was not discussed but the quantization noise of scenario 2 was assumed.

a) What is the quantization noise if the breakpoints of Scenario 1 is used?
b) What is the reason that the breakpoints were not discussed when defining the quantization noise of an ideal ADC?




**Scenario 1**




**Scenario 2**

Problem 10 An EXCEL data sheet is attached. Assume the entries in the spreadsheet are break-points for an ADC.

a) What is the INL and DNL?

b) Determine the SFDR, the THD, and the ENOB if a low-frequency sinusoid is applied to the input.